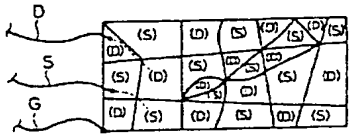
(54) MOS TRANSISTOR
(11) 6-37311 (A) (43) 10.2.1994 (19) JP
(21) Appl. No. 4-210779 (22) 15.7.1992
(71) ROHM CO LTD (72) TAMOTSU SUZUKI(1)
(51) Int. Cl⁵. H01L29/784

PURPOSE: To increase ability to drive a MOS transistor without increasing the area of a chip.

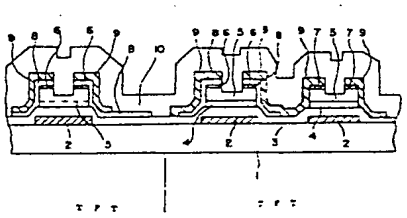
CONSTITUTION: A linear channel region is arranged in the form of lattice and mesh (See a bold line in Figure). And then two regions are consituted by being divided with the channel region so as to adjacently contain it therebetween, one of which is formed to act as a source region (S) and the other of which is formed to act as a drain region (D). Thereby, the length of whole channels is increased to increase ability to drive even with a chip in same size.



(54) THIN-FILM SEMICONDUCTOR DEVICE AND MANUFACTURE THEREOF
(11) 6-37313 (A) (43) 10.2.1994 (19) JP
(21) Appl. No. 4-189467 (22) 16.7.1992
(71) HITACHI LTD (72) KIKUO ONO
(51) Int. Cl⁵. H01L29/784,G02F1/136

PURPOSE: To provide a semiconductor device in which an N-type TFT for a picture element part and an N-type TFT and a P-type TFT of a complementary (C) type circuit for driving the former are built in the same substrate, and also to provide the manufacture thereof without increasing the number of a photo-resist process more than that in a conventional N-type circuit.

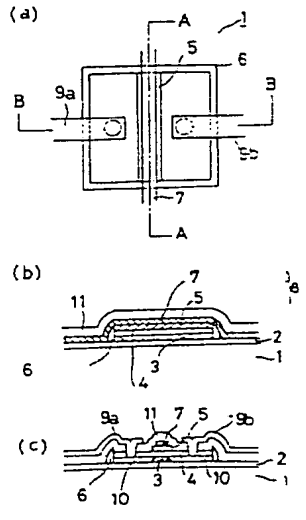
CONSTITUTION: A gate electrode 2, a gate insulating film 3 and silicon layers (5, 4 & 5) for each TFT are sequentially formed on a transparent substrate 1, and after N-type impurities are doped thereinto, photo etching is applied for the division of the substrate into first through third islands to make a semiconductor layer for each TFT so that the first island is formed to act as an N-type semiconductor layer 5 for a picture element part and the second island is formed to act as an N-type semiconductor layer 6 for a C-type circuit, and then a film of ITO for a picture element electrode 8 is so accumulated as to cover only the first and the second islands. After that, doping is performed in such a manner that the concentration of P-type impurities becomes higher than that of N-type impurities to form the third island in a P-type semiconductor layer for the C-type circuit and then the source/drain electrodes 9 for each TFT and also a protective film 10 are formed.



(54) THIN-FILM TRANSISTOR AND MANUFACTURE THEREOF
(11) 6-37314 (A) (43) 10.2.1994 (19) JP
(21) Appl. No. 4-189334 (22) 16.7.1992
(71) SHARP CORP (72) KEIJI TARUI(2)
(51) Int. Cl⁵. H01L29/784

PURPOSE: To facilitate the formation of a gate overlapping LDD by forming a gate electrode in two-layer structure of an upper layer and a lower layer and performing the ion implantation of impurities with both electrodes being used for a mask without equalling the width of both electrodes.

CONSTITUTION: A gate electrode 5 of a lower layer is worked for a predetermined shape with a reactive ion etcher. Then, the width of an electrode for the gate electrode 5 of a lower layer is made to be 5μm. After that, a polysilicon film to act as a gate electrode 7 of an upper layer is formed on the whole surface of a glass substrate 1 including the electrode 5 of a lower layer. And then the width of an electrode for the gate electrode 7 of an upper layer is so worked as to become 3μm with the center line of the electrode width of the gate electrode 5 of a lower layer being aligned with that of the gate electrode 7 of an upper layer. Next, P-type ion implantation is so performed as to form a high concentration region in a gate electrode 6 and at the same time to form an impurity region 10 having an LDD structure in the polysilicon film. Since the gate electrode width of an upper and a lower layer is not the same, a gate overlapping LDD structure may be easily formed with once implantation of impurity ions being performed by using the gate electrode of an upper and a lower layer for a mask.



1: glass electrode (insulating substrate). 3: polysilicon layer. 4: SiO_2 film (gate insulating film). 10: impurity diffused layer